9. (NEW) The interrupt request controller recited in claim 5 wherein the programmable assertion sense and/or assertion type section includes for each one of the interrupt logic signals, an interrupt type register for storing a bit representative of whether the logic state of the interrupt logic signal should remain as an edge or be converted to a level.

REMARKS

The above-identified patent application has been amended and reconsideration and re-examination are hereby requested.

Before discussing the claims and how they distinguish over the cited art, perhaps it might be helpful to review features of applicant's invention.

In accordance with a **first** feature of the invention, reference is made to FIG. 6A. As shown therein there are two masks: a source mask register section 323 and a second mask section 325. As described in the patent application:

> More particularly, the Int4 through Int0 mask registers in section 325 select which interrupt bits from the source mask register 323 participate on a given level. Each Intx mask is OR-reduced in OR gate section 327 to arrive at the primary IRQnp<4..0> outputs. These outputs may be used where desired to change the flow in execution of a program, for example.

This feature is the subject of claim 1 and is also included in claim 5.

In accordance with a **second** feature, as pointed out in the patent application:

> More particularly, each bit is fed to an interrupt type register 314, an exemplary one thereof being shown in FIG. 8. ***The interrupt type register 314 determines whether the interrupt IRQ should be an edge (leading or trailing edge) or remain as a level***. More particularly, the register 314 includes a multiplexer 316. The multiplexer 316 has one port, port A, fed by the interrupt request IRQ and the other input, port B, fed by an edge logic 318. The edge logic 318 includes an OR gate 320. One input to the OR gate is fed by the interrupt request IRQ through an AND gate 319 and register 321, as indicated, and the

other input to the OR gate 320 is fed by a clear signal through AND gate 322, as indicated. The output of the OR gate is fed to a register 330. The output of register 330 is fed to the B input of multiplexer 316. A register 326 is provided to produce the port select signal for the multiplexer 316. ***If a logic 1 is stored in the register 326, the A port is coupled to the output of the multiplexer 316 thereby selected a level as in interrupt request type. On the other hand, if a logic 1 is stored in the register 326 the output of the edge logic 318 is coupled to the output of the multiplexer 316.***

More particularly, in response to a clock pulse, register 321 stores the level of the interrupt fed thereto. The stored level is fed to the inverted input of AND gate 319. Thus, AND gate 319 compares the level of the present interrupt with the level of the previous interrupt (i.e., the level of the interrupt on the previous clock). If they differ, a logic 1 is asserted and becomes stored in register 330. The stored logic 1 in register 330 is then fed back to the non-inverting input of AND gate 322. The output of AND gate 322, in the absence of a clear signal from the microprocessor interface 52 (FIG. 2) passes through OR gate 320 where it remains until the presence of a clear signal. Thus the clear opens the feedback path. ***Thus, in response to an edge (i.e., leading or trailing edge) of the interrupt signal, such edge is converted into a level which appears at the output of register 330 (i.e., at the B input of selector 316.***

The interrupt requests produced by the interrupt type register section 312 is fed to a current interrupt register 321. The contents of the current interrupt register may be observed for testing or, in operation, for polling, for example. These contents are also fed to a source mask 323 wherein any one of the 32 bits may be masked as desired. (Emphasis added)

This feature is the subject of claims 2-9.

Referring now to the claims:

Claim 1 points out that the interrupt section is fed by the programmable mask section for coupling unmasked ones of the interrupt signals to a plurality of outputs selectively in accordance with a predetermined criteria, such predetermined criteria being established by a second mask. (Emphasis added). It is respectfully submitted that Temple, U. S. Patent No. 5,875,342), does not describe or suggests " an interrupt section [is] fed by the programmable mask section for coupling unmasked ones of the interrupt signals to a plurality of outputs selectively in accordance with a predetermined criteria, such predetermined criteria being established by a second mask".

Claim 2 points out that an interrupt request controller for processing a plurality of interrupt logic signals, such controller comprises a programmable section fed by the interrupt

signals, for selecting ***assertion sense*** and/or ***assertion type*** of each one of the interrupt signals. It is respectfully submitted that Temple, U. S. Patent No. 5,875,342), does not describe or suggests a programmable section fed by the interrupt signals, for selecting ***assertion sense*** and/or ***assertion type*** of each one of the interrupt signals.

Claim 3 points out that a programmable section is fed the interrupt signals, for storing a bit for each one of the interrupt logic ***signals representative of whether the logic state of the interrupt logic signal should be, or should not be, inverted and for producing a corresponding output logic interrupt signal in accordance therewith***. It is respectfully submitted that Temple, U. S. Patent No. 5,875,342), does not describe or suggests a programmable section is fed the interrupt signals, for storing a bit for each one of the interrupt logic ***signals representative of whether the logic state of the interrupt logic signal should be, or should not be, inverted and for producing a corresponding output logic interrupt signal in accordance therewith.***

Claim 4 points out that a programmable section is fed the interrupt signals, for storing a bit for each one of the interrupt logic signals representative of ***whether the logic state of the interrupt logic signal should be an edge or remain as a level and for producing a corresponding output logic interrupt signal in accordance therewith***. Examiner's statement that such is described in Temple is not understood. This feature is described above in this response. Applicant find s no reference in Temple to a programmable section is fed the interrupt signals, for storing a bit for each one of the interrupt logic signals representative of ***whether the logic state of the interrupt logic signal should be an edge or remain as a level and for producing a corresponding output logic interrupt signal in accordance therewith***.

Claim 5 points out an interrupt request controller is provided for processing a plurality of interrupt logic signals. The controller comprises: a programmable section fed by the interrupt signals, for selecting ***assertion sense*** and/or ***assertion type*** of each one of the interrupt signals; programmable bit masking section coupled to the programmable assertion sense/assertion type section, adapted to mask selected ones of the interrupt signals; and an interrupt section fed by the programmable mask section for coupling unmasked ones of the interrupt signals to a plurality

of outputs selectively in accordance with a predetermined criteria, ***such predetermined criteria being established by a second mask***. As noted above, it is respectfully submitted that these two features are not described in Temple.

Claim 6 points out that the programmable assertion sense and/or assertion type section includes for each one of the interrupt logic signals an interrupt sense register for storing a bit representative of whether the logic state of the interrupt logic signal should be, or should not be, inverted. As noted above, it is respectfully submitted that these two features are not described in Temple.

Claims 7, 8 and 9 point out that the programmable assertion sense and/or assertion type section includes for each one of the interrupt logic signals, an interrupt type register for storing a bit representative of ***whether the logic state of the interrupt logic signal should remain as an edge or be converted to a level***. As noted above, it is respectfully submitted that these two features are not described in Temple.

In the event any additional fee is required, please charge such amount to Patent and Trademark Office Deposit Account No. 50-0845.

Respectfully submitted,

12/12/02
Date

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Attachment: Claim Mark Up Sheets
EMC2-033PUS-response to final office action dated 09_24_02.doc

COMPARISON CLAIMS

2. (Amended) An interrupt request controller for processing a plurality of interrupt logic signals, such controller, comprising:

a programmable bit masking section fed by the interrupt logic signals, adapted to mask selected ones of the interrupt signals;

~~a~~ an interrupt ~~priority~~ section fed by the programmable mask section for coupling unmasked ones of the interrupt signals to a plurality of outputs selectively in accordance with a predetermined ~~priority~~ criteria, such predetermined criteria being established by a second mask..

2. An interrupt request controller for processing a plurality of interrupt logic signals, such controller, comprising:

a programmable section fed by the interrupt signals, for selecting assertion sense and/or assertion type of each one of the interrupt signals.

3. An interrupt request controller for processing a plurality of interrupt logic signals, such controller, comprising:

a programmable section fed the interrupt signals, for storing a bit for each one of the interrupt logic signals representative of whether the logic state of the interrupt logic signal should be, or should not be, inverted and for producing a corresponding output logic interrupt signal in accordance therewith.

4. (Amended) An interrupt request controller for processing a plurality of interrupt logic signals, such controller, comprising:

a programmable section fed the interrupt signals, for storing a bit for each one of the interrupt logic signals representative of whether the logic state of the interrupt logic signal

should ~~remain as~~ be an edge or remain as a ~~be converted to a~~ level and for producing a corresponding output logic interrupt signal in accordance therewith.

5. An interrupt request controller for processing a plurality of interrupt logic signals, such controller, comprising:

a programmable section fed by the interrupt signals, for selecting assertion sense and/or assertion type of each one of the interrupt signals;

a programmable bit masking section coupled to the programmable assertion sense/assertion type section, adapted to mask selected ones of the interrupt signals;

~~a~~ an interrupt ~~priority~~ section fed by the programmable mask section for coupling unmasked ones of the interrupt signals to a plurality of outputs selectively in accordance with a predetermined ~~priority~~ criteria, such predetermined criteria being established by a second mask.

6. The interrupt request controller recited in claim 5 wherein the programmable assertion sense and/or assertion type section includes for each one of the interrupt logic signals an interrupt sense register for storing a bit representative of whether the logic state of the interrupt logic signal should be, or should not be, inverted.

7. The interrupt request controller recited in claim 6 wherein the programmable assertion sense and/or assertion type section includes for each one of the interrupt logic signals, an interrupt type register for storing a bit representative of whether the logic state of the interrupt logic signal should remain as an edge or be converted to a level.

8. (NEW) The interrupt request controller recited in claim 5 wherein the programmable assertion sense and/or assertion type section includes for each one of the interrupt logic signals, an interrupt type register for storing a bit representative of whether the logic state of the interrupt logic signal should remain as an edge or be converted to a level.

9. (NEW) The interrupt request controller recited in claim 5 wherein the programmable assertion sense and/or assertion type section includes for each one of the interrupt logic signals, an interrupt type register for storing a bit representative of whether the logic state of the interrupt logic signal should remain as an edge or be converted to a level.